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# PALM INTRANET

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## Inventor Name Search Result

Your Search was:

Last Name = MOLL

First Name = LAURENT

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">09264347</a>	6753878	150	03/08/1999	PARALLEL PIPELINED MERGE ENGINES	MOLL, LAURENT
<a href="#">10356323</a>	7403525	150	01/31/2003	EFFICIENT ROUTING OF PACKET DATA IN A SCALABLE PROCESSING RESOURCE	MOLL, LAURENT
<a href="#">10356324</a>	7346078	150	01/31/2003	PROCESSING OF RECEIVED DATA WITHIN A MULTIPLE PROCESSOR DEVICE	MOLL, LAURENT
<a href="#">10356348</a>	Not Issued	41	01/31/2003	Transmitting data from a plurality of virtual channels via a multiple processor device	MOLL, LAURENT
<a href="#">10356390</a>	Not Issued	61	01/31/2003	Multiple processor integrated circuit having configurable packet-based interfaces	MOLL, LAURENT
<a href="#">10356661</a>	Not Issued	41	01/31/2003	Packet data service over hyper transport link(s)	MOLL, LAURENT
<a href="#">10684871</a>	7366092	150	10/14/2003	HASH AND ROUTE HARDWARE WITH PARALLEL ROUTING SCHEME	MOLL, LAURENT
<a href="#">10684909</a>	7131020	150	10/14/2003	DISTRIBUTED COPIES OF CONFIGURATION INFORMATION USING TOKEN RING	MOLL, LAURENT
<a href="#">10684915</a>	7272151	150	10/14/2003	CENTRALIZED SWITCHING FABRIC SCHEDULER SUPPORTING SIMULTANEOUS UPDATES	MOLL, LAURENT
<a href="#">10684953</a>	Not Issued	93	10/14/2003	HYPERTRANSPORT EXCEPTION DETECTION AND PROCESSING	MOLL, LAURENT
<a href="#">10685129</a>	7243172	150	10/14/2003	FRAGMENT STORAGE FOR DATA ALIGNMENT AND MERGER	MOLL, LAURENT
<a href="#">10685376</a>	7218638	150	10/14/2003	SWITCH OPERATION SCHEDULING MECHANISM WITH CONCURRENT CONNECTION AND QUEUE	MOLL, LAURENT

				SCHEDULING	
<a href="#">10864609</a>	Not Issued	161	06/09/2004	Parallel pipelined merge engines	MOLL, LAURENT
<a href="#">10941172</a>	<a href="#">7404044</a>	150	09/15/2004	SYSTEM AND METHOD FOR DATA TRANSFER BETWEEN MULTIPLE PROCESSORS	MOLL, LAURENT
<a href="#">11781726</a>	Not Issued	25	07/23/2007	VIRTUAL CORE MANAGEMENT	MOLL, LAURENT
<a href="#">11786275</a>	Not Issued	51	04/11/2007	Receiving data from virtual channels	MOLL, LAURENT
<a href="#">12109459</a>	Not Issued	25	04/25/2008	Hash and Route Hardware with Parallel Routing Scheme	MOLL, LAURENT
<a href="#">60331789</a>	Not Issued	159	11/20/2001	Packet data service over hyper transport link(s)	MOLL, LAURENT
<a href="#">60344713</a>	Not Issued	159	12/24/2001	Multi-function hypertransport devices	MOLL, LAURENT
<a href="#">60348717</a>	Not Issued	159	01/14/2002	Hyper transport coupled distributed system host	MOLL, LAURENT
<a href="#">60348777</a>	Not Issued	159	01/14/2002	Multi-function hypertransport devices	MOLL, LAURENT
<a href="#">60419031</a>	Not Issued	160	10/16/2002	Processing of received data within a multiple processor device	MOLL, LAURENT
<a href="#">60419040</a>	Not Issued	159	10/16/2002	Transmitting data from a plurality of virtual channels via a multiple processor device	MOLL, LAURENT
<a href="#">60419041</a>	Not Issued	159	10/16/2002	Packet data service over hypertransport links	MOLL, LAURENT
<a href="#">60419042</a>	Not Issued	159	10/16/2002	Efficient routing of packet data in a scalable processing resource	MOLL, LAURENT
<a href="#">60520166</a>	Not Issued	159	11/14/2003	Hyper transport/SPI-4 interface supporting configurable deskewing	MOLL, LAURENT
<a href="#">10269666</a>	<a href="#">6912602</a>	150	10/11/2002	SYSTEM HAVING TWO OR MORE PACKET INTERFACES, A SWITCH, AND A SHARED PACKET DMA CIRCUIT	MOLL, LAURENT R.
<a href="#">10269922</a>	<a href="#">7206879</a>	150	10/11/2002	SYSTEMS USING MIX OF PACKET, COHERENT, AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS	MOLL, LAURENT R.
<a href="#">10270016</a>	<a href="#">7227870</a>	150	10/11/2002	SYSTEMS INCLUDING PACKET INTERFACES, SWITCHES, AND PACKET DMA CIRCUITS FOR SPLITTING AND MERGING PACKET STREAMS	MOLL, LAURENT R.
<a href="#">10270029</a>	<a href="#">6748479</a>	150	10/11/2002	SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND	MOLL, LAURENT R.

				PACKET TRAFFIC	
<a href="#">10439297</a>	<a href="#">6941440</a>	150	05/15/2003	ADDRESSING SCHEME SUPPORTING VARIABLE LOCAL ADDRESSING AND VARIABLE GLOBAL ADDRESSING	MOLL, LAURENT R.
<a href="#">10439343</a>	<a href="#">7340546</a>	150	05/15/2003	ADDRESSING SCHEME SUPPORTING FIXED LOCAL ADDRESSING AND VARIABLE GLOBAL ADDRESSING	MOLL, LAURENT R.
<a href="#">10675745</a>	Not Issued	61	09/30/2003	Management of received data within host device using linked lists	MOLL, LAURENT R.
<a href="#">10684872</a>	<a href="#">7096305</a>	150	10/14/2003	PERIPHERAL BUS SWITCH HAVING VIRTUAL PERIPHERAL BUS AND CONFIGURABLE HOST BRIDGE	MOLL, LAURENT R.
<a href="#">10684988</a>	<a href="#">7380018</a>	150	10/14/2003	PERIPHERAL BUS TRANSACTION ROUTING USING PRIMARY AND NODE ID ROUTING INFORMATION	MOLL, LAURENT R.
<a href="#">10684989</a>	<a href="#">7313146</a>	150	10/14/2003	TRANSPARENT DATA FORMAT WITHIN HOST DEVICE SUPPORTING DIFFERING TRANSACTION TYPES	MOLL, LAURENT R.
<a href="#">10684998</a>	<a href="#">7319702</a>	150	10/14/2003	APPARATUS AND METHOD TO RECEIVE AND DECODE INCOMING DATA AND TO HANDLE REPEATED SIMULTANEOUS SMALL FRAGMENTS	MOLL, LAURENT R.
<a href="#">10685231</a>	Not Issued	71	10/14/2003	Apparatus and method to receive and align incoming data in a buffer to expand data width by utilizing a single write port memory device	MOLL, LAURENT R.
<a href="#">10742060</a>	<a href="#">7490187</a>	150	12/20/2003	HYPERTRANSPORT/SPI-4 INTERFACE SUPPORTING CONFIGURABLE DESKEWING	MOLL, LAURENT R.
<a href="#">10861624</a>	<a href="#">6941406</a>	150	06/04/2004	SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND PACKET TRAFFIC	MOLL, LAURENT R.
<a href="#">11069313</a>	Not Issued	161	03/01/2005	System having two or more packet interfaces, a switch, and a shared packet DMA circuit	MOLL, LAURENT R.
<a href="#">11146449</a>	Not Issued	161	06/07/2005	System having interfaces and switch that separates coherent and packet traffic	MOLL, LAURENT R.
<a href="#">11146450</a>	Not	161	06/07/2005	Addressing scheme supporting	MOLL, LAURENT

	Issued			variable local addressing and variable global addressing	R.
<a href="#">11279880</a>	Not Issued	95	04/15/2006	IMPROVED PREFETCH HARDWARE EFFICIENCY VIA PREFETCH HINT INSTRUCTIONS	MOLL, LAURENT R.
<a href="#">11351058</a>	<a href="#">7412570</a>	150	02/09/2006	SMALL AND POWER- EFFICIENT CACHE THAT CAN PROVIDE DATA FOR BACKGROUND DMA DEVICES WHILE THE PROCESSOR IS IN A LOW-POWER STATE	MOLL, LAURENT R.
<a href="#">11351070</a>	<a href="#">7516274</a>	150	02/09/2006	POWER CONSERVATION VIA DRAM ACCESS REDUCTION	MOLL, LAURENT R.
<a href="#">11416872</a>	Not Issued	41	05/02/2006	System and method for optimizing a memory controller	MOLL, LAURENT R.
<a href="#">11435528</a>	Not Issued	41	05/17/2006	System and method for processing instructions in a computer system	MOLL, LAURENT R.
<a href="#">11446897</a>	Not Issued	71	06/05/2006	Peripheral bus switch having virtual peripheral bus and configurable host bridge	MOLL, LAURENT R.
<a href="#">11450103</a>	Not Issued	30	06/09/2006	System and method for conserving power	MOLL, LAURENT R.

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